REMARKS

Claims 1, 4-11 and 14-21 remain pending herein. Claims 2 and 13 have been canceled, the subject matter thereof being incorporated into claim 1. In addition, claim 20 has been rewritten to be in independent form.

1. Withdrawal of the rejections stated in the Office Action dated August 24, 2005 is acknowledged and appreciated by Applicants.

2. Claims 1, 2, 4-9, 13-19 and 21 were rejected under §103 over Thilderkvist et al. in view of Kumar et al. This rejection is respectfully traversed for the following reasons.

The claimed invention is drawn to a semiconductor processing component comprising SiC, having an outer surface portion that consists essentially of CVD-SiC, and has a surface impurity level of not greater than 2 times a bulk impurity level. The claimed invention has been developed based upon discovery by the Applicants of a particularly surprising artifact of CVD-SiC processing. Namely, Applicants have discovered that during formation of what is conventionally understood to be a high purity CVD-SiC coating on semiconductor processing components such as wafer boats, the CVD-SiC coating has an attendant spike in impurities at the outer surface, which may extend several microns into the CVD-SiC coating. Particular impurity profiles are shown in FIGs. 2-4 for various as-deposited CVD-SiC coatings, which notably show impurity levels at the outer surface greater than 100X, such as about 1000X, the bulk impurity level. In order to improve purity, an outer target portion of the CVD-SiC coating is removed, generally through an oxidation and etch process. Through one or several oxidation and etch procedures, the outer portion of the CVD-SiC layer that is impurity enriched is removed such that the outer surface portion has a surface impurity level that is not greater than 2 times a bulk impurity level.

As mentioned in paragraph 45 of the present specification, the mechanism or root cause for impurity enrichment at the surface is not well understood, but may relate to impurity migration from the surface of the underlying substrate during CVD-SiC deposition processing, or impurity segregation from the interior of the film to the surface during cooling.

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Thilderkvist et al. discloses a process for purifying a substrate such as a processing chamber that has been contaminated with metal, for example. Thilderkvist et al. discloses a process in which a sacrificial layer, such as silicon, is deposited on a surface of a processing chamber, permitting diffusion of contaminants into the silicon layer. The silicon layer and the trapped contaminants are then removed, leaving behind a cleaner surface.

While Thilderkvist et al. evidently teaches the partial purification of an outer surface portion of a processing chamber for semiconductor manufacture, the process of Thilderkvist et al. cannot possibly result in the level of purity as presently claimed. Particularly, the disclosure of Thilderkvist et al. is principally focused upon removal of contaminants following a known contamination process, such as metal contamination during packaging or handling with metal parts or tools. See paragraph bridging columns 6 and 7 of Thilderkvist et al. Thilderkvist et al. does not disclose or even remotely recognize the intrinsic impurity spike of the surface of an as-deposited CVD-SiC film. As noted above, this intrinsic spike is generally at least 100X and ranging up to 1000X the level of impurities in the bulk of the component. The claimed invention achieves notable impurity reduction through a *removal* process, in which a portion of the CVD-SiC material is removed. In contrast, Thilderkvist et al. merely teaches a diffusion process, and not removal of an outer surface portion that is rich in impurities. Based upon the teaching of Thilderkvist et al., Applicants submit that the sacrificial layer formation and impurity diffusion, cannot possible result in 1000X, let alone 100X reduction in impurity levels to achieve an outer surface having an impurity level not greater than 2X a bulk impurity level, enabled by an oxidation/removal process.

The secondary reference to Kumar et al. has been relied upon for disclosure of a Si/SiC based composition. However, Kumar et al. fail to cure the deficiencies of Thilderkvist et al. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103 rejection over Thilderkvist et al. in view of Kumar et al.

3. Claims 10 and 11 were rejected under §103 in further view of Bosch. Applicants submit that Bosch fails to overcome the deficiencies of Thilderkvist et al. and Kumar et al. discussed above, and accordingly, withdrawal of this rejection is respectfully requested as well.

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4. Claim 20 was rejected under §103 in further view of Goldstein et al. Similarly, Goldstein et al. fail to cure the deficiencies of Thilderkvist et al. and Kumar et al. Accordingly, withdrawal of this rejection is respectfully requested as well.

Applicants respectfully submit that the present application is now in condition for allowance. Accordingly, the Examiner is requested to issue a Notice of Allowance for all pending claims.

Should the Examiner deem that any further action by the Applicants would be desirable for placing this application in even better condition for issue, the Examiner is requested to telephone the Applicants' undersigned representative at the number below.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-3797.

Respectfully submitted,

7/3/06
Date

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